Future of the ATLAS Liquid Argon Calorimeter

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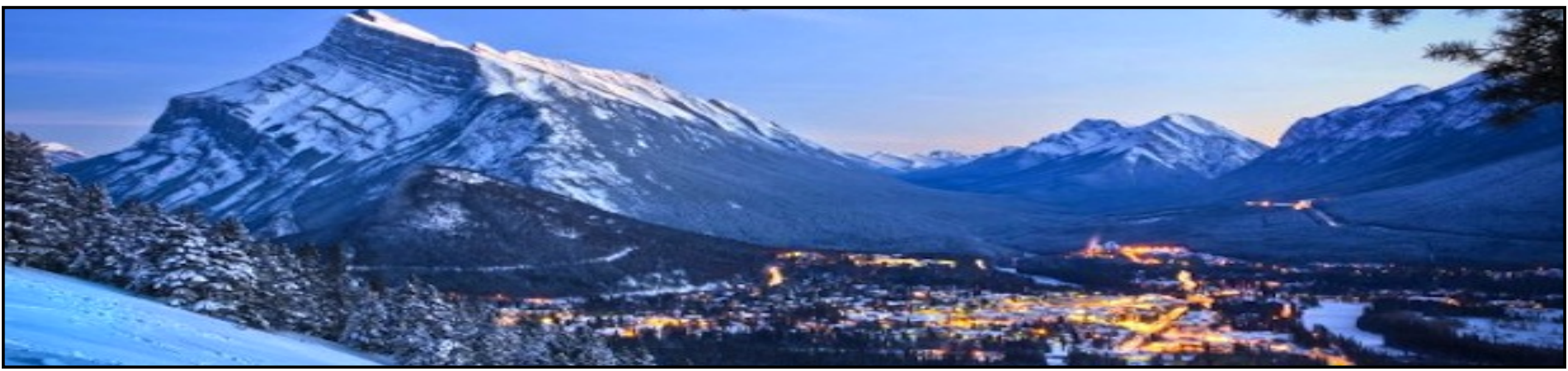
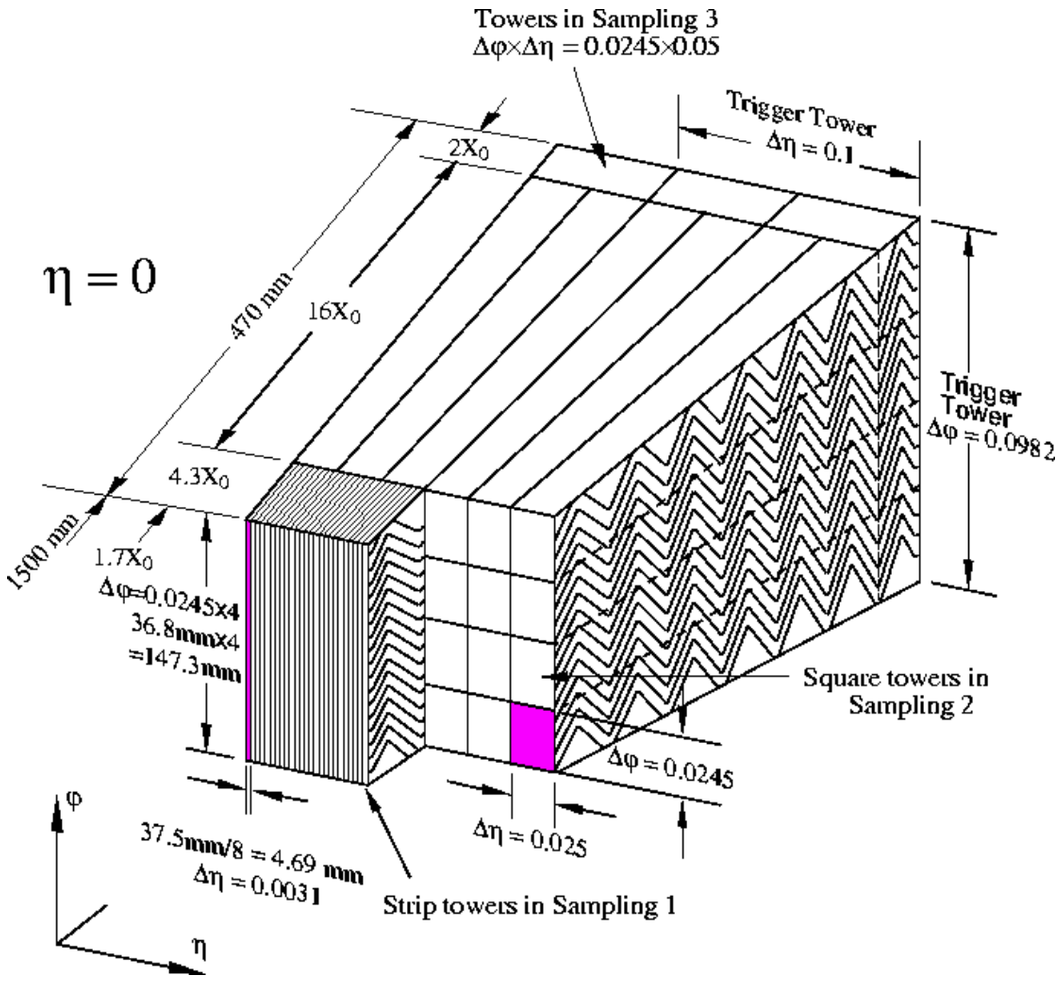
University of Victoria

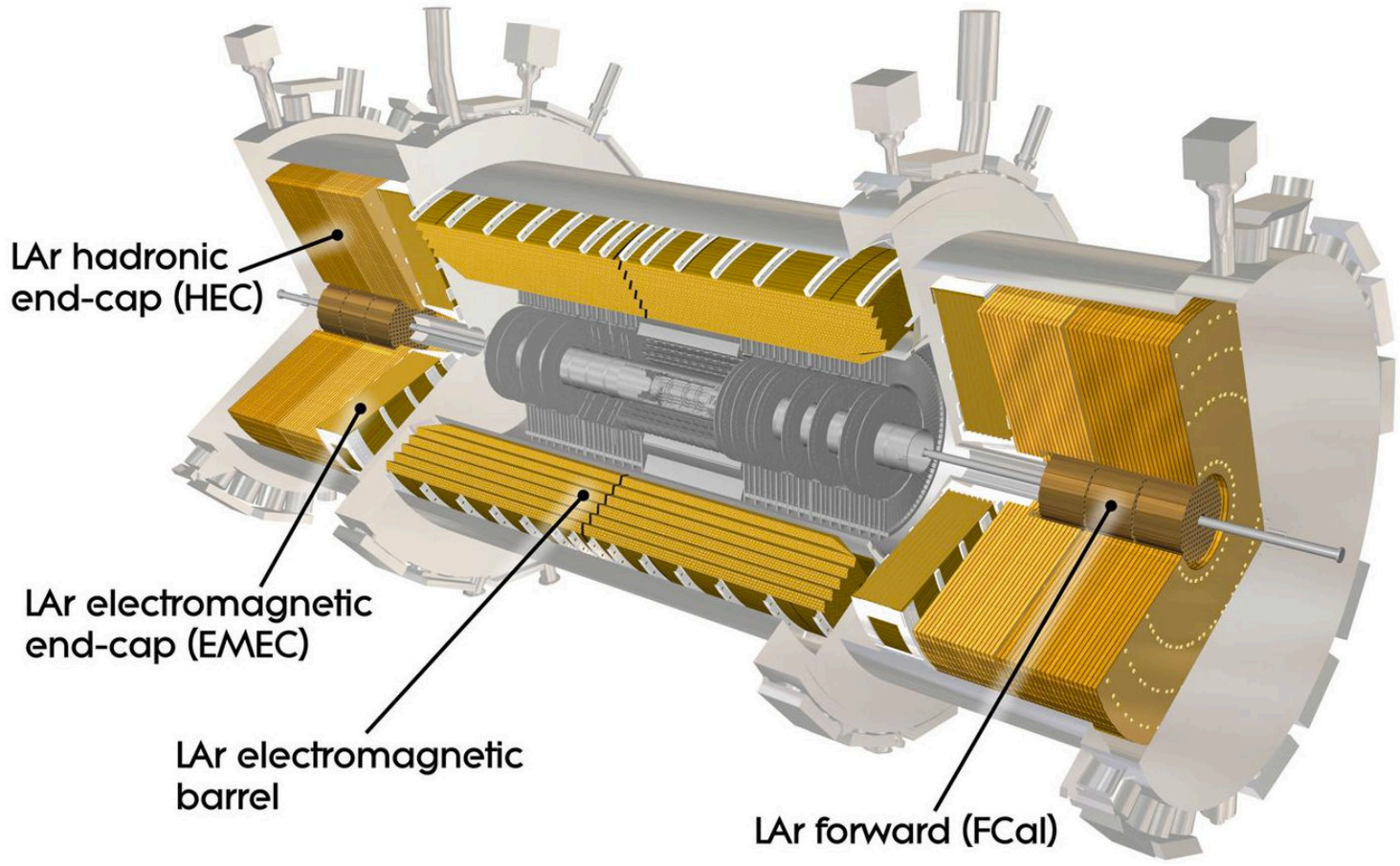


Liquid Argon Calorimeter

Sampling Calorimeters

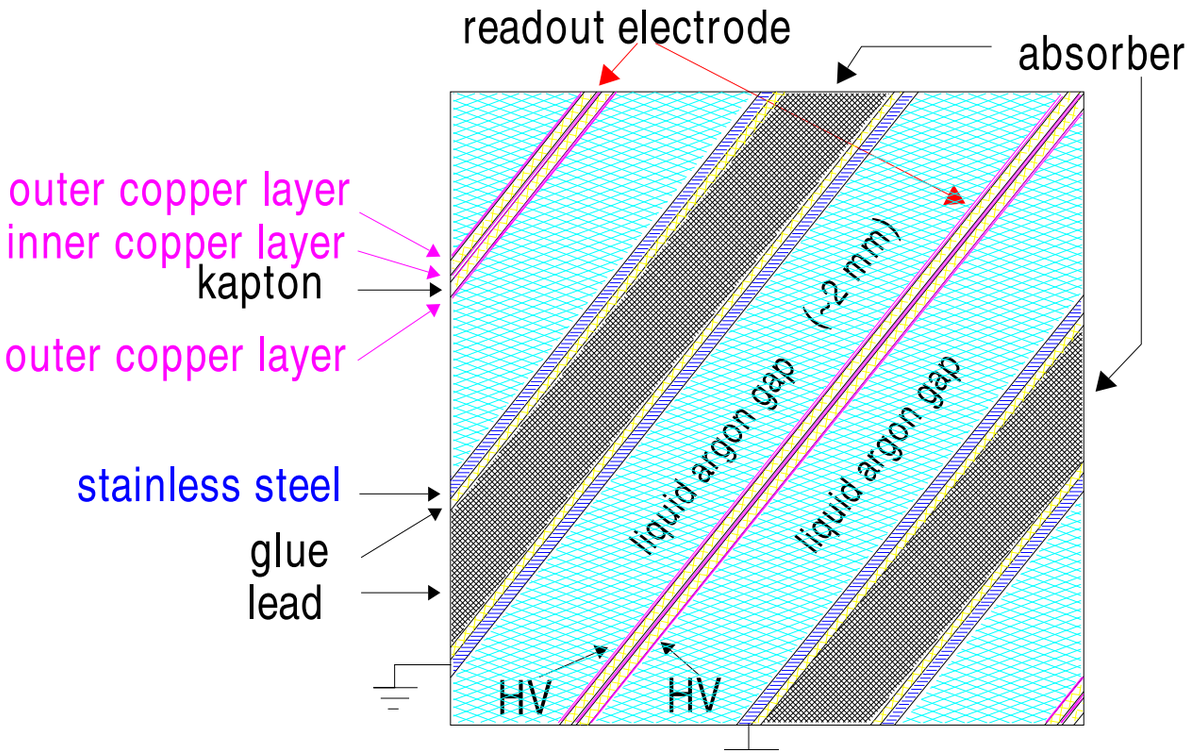
- **EMB**: LAr - Lead, $|\eta| < 1.475$
- **EMEC**: LAr - Lead, $1.375 < |\eta| < 3.2$
- **HEC**: LAr - Copper, $1.5 < |\eta| < 3.2$
- **FCAL**: LAr - Copper, $3.1 < |\eta| < 4.9$
  and LAr - Tungsten



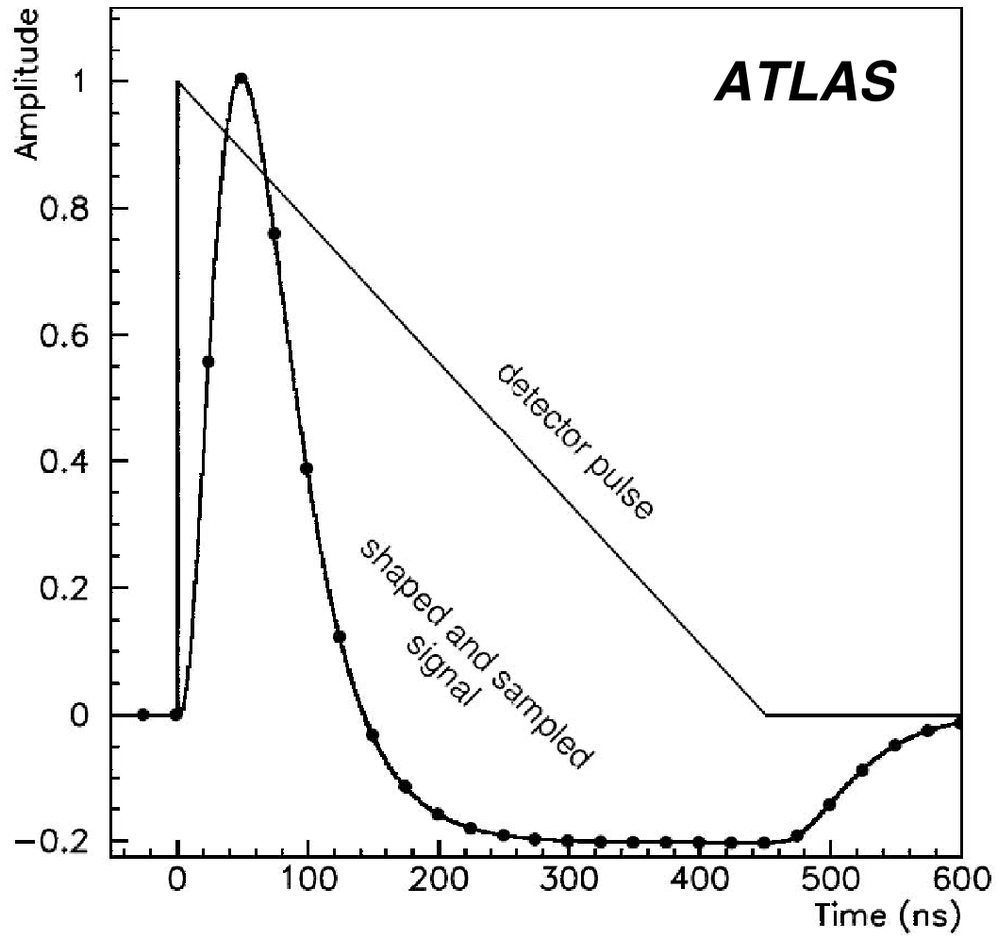


- 182,500 channels.
- The layers of each module have different granularities.
- Largest fraction of energy deposited in middle layer. (EM Calo)
- Fine granularity used to reconstruct incident particle's direction.

Pulse Shaping



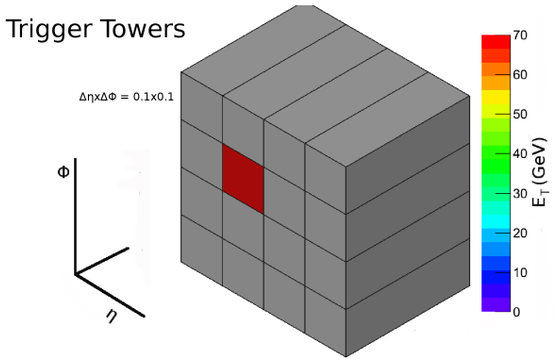
- High energy particles shower in the calorimeter, ionizing the LAr.
- HV readout electrodes placed between grounded absorbers.
- Drift gap of 2.1 mm corresponding to electron drift time of 450 ns (for EM Calo)



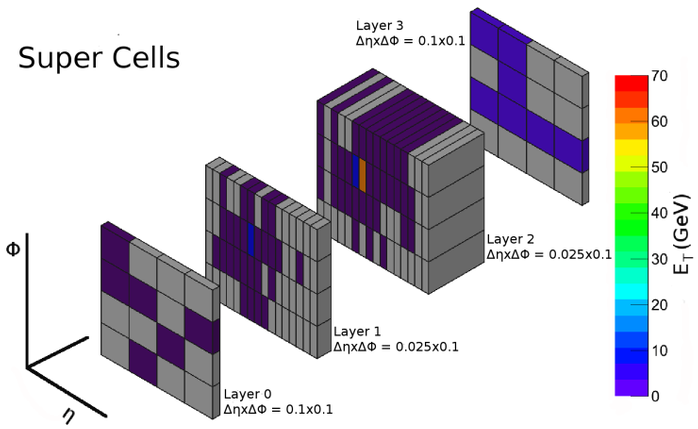
- Drift electrons induce a triangular pulse, amplitude proportional to deposited energy.
- Pulse passed through Bipolar CR -$(RC)^2$ filter. (Baseline shaping time of 13 ns)
- 25 nano-second sampling.

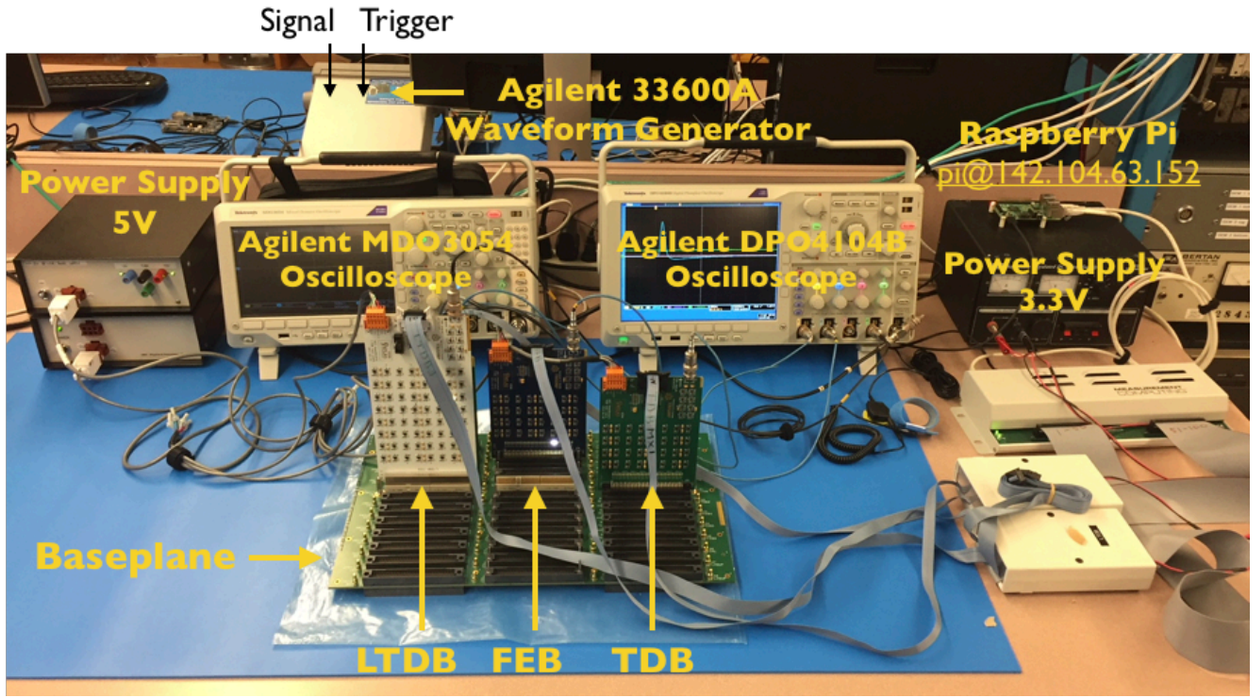
Phase-I Upgrades

Improvements to the LAr Calorimeter are currently under way, with Canadian institutes actively involved:



Comparison of energy deposits for a 70 GeV electron.

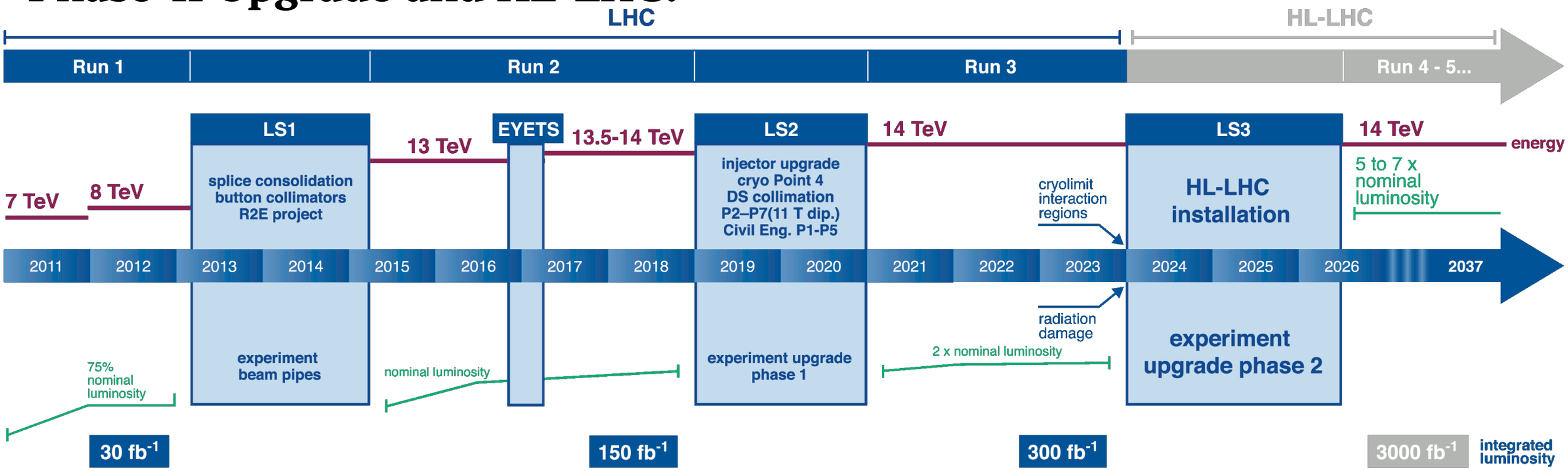


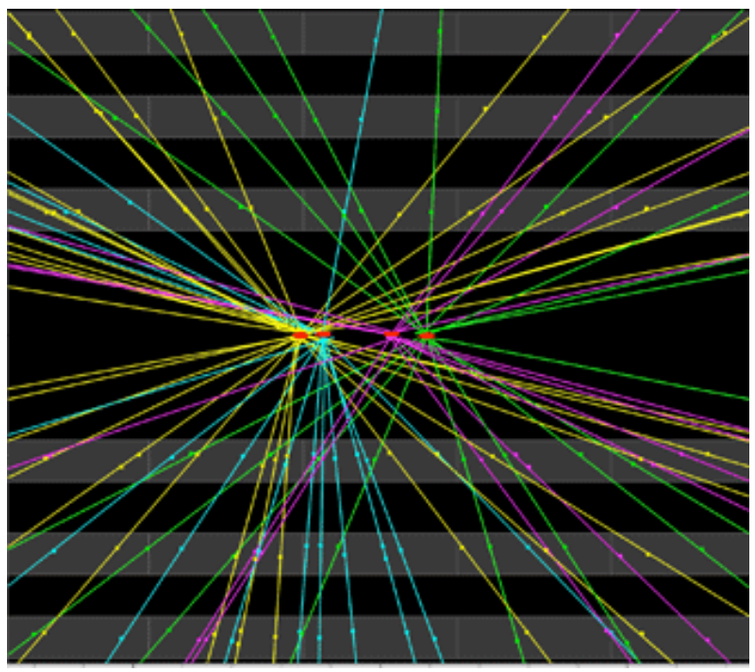


- For Phase-I Upgrade calorimeter signal is split between new “SuperCell” based LAr Trigger Digitizer Boards (LTDB) and legacy Tower Builder Boards (TBB).
- SuperCells are groupings of calorimeter cells offering:
  - Finer Granularity
  - Layer Information
- Will improve trigger efficiencies and reduce trigger rates while maintaining or even lowering trigger thresholds.
- Splitting between the two trigger electronics requires new baseplanes.
- Baseplanes for the HEC were designed at TRIUMF and tested at the University of Victoria.

High Luminosity LHC

Phase-II Upgrade and HL-LHC:





- $7.5 \cdot 10^{-34}$ $cm^{-2}s^{-1}$ peak luminosity.
- 25 ns bunch spacing (40 MHz)
- Expected integrated luminosity of 4000 fb^{-1} (over ~12 years)
- Up to 200 average minimum bias events per bunch crossing
- Increased radiation damage to detector

Upgrade Motivation

Technical Motivations:

Preserving physics reach (ie Higgs) for higher data taking rates requires updated triggers:

- Current readout electronics are incompatible with new Trigger System. Upgraded triggers require higher trigger rate (1MHz), longer latency, and higher granularity calorimeter information.
- Existing front-end electronics will reach the limit of their radiation tolerance before the end of the HL-LHC.

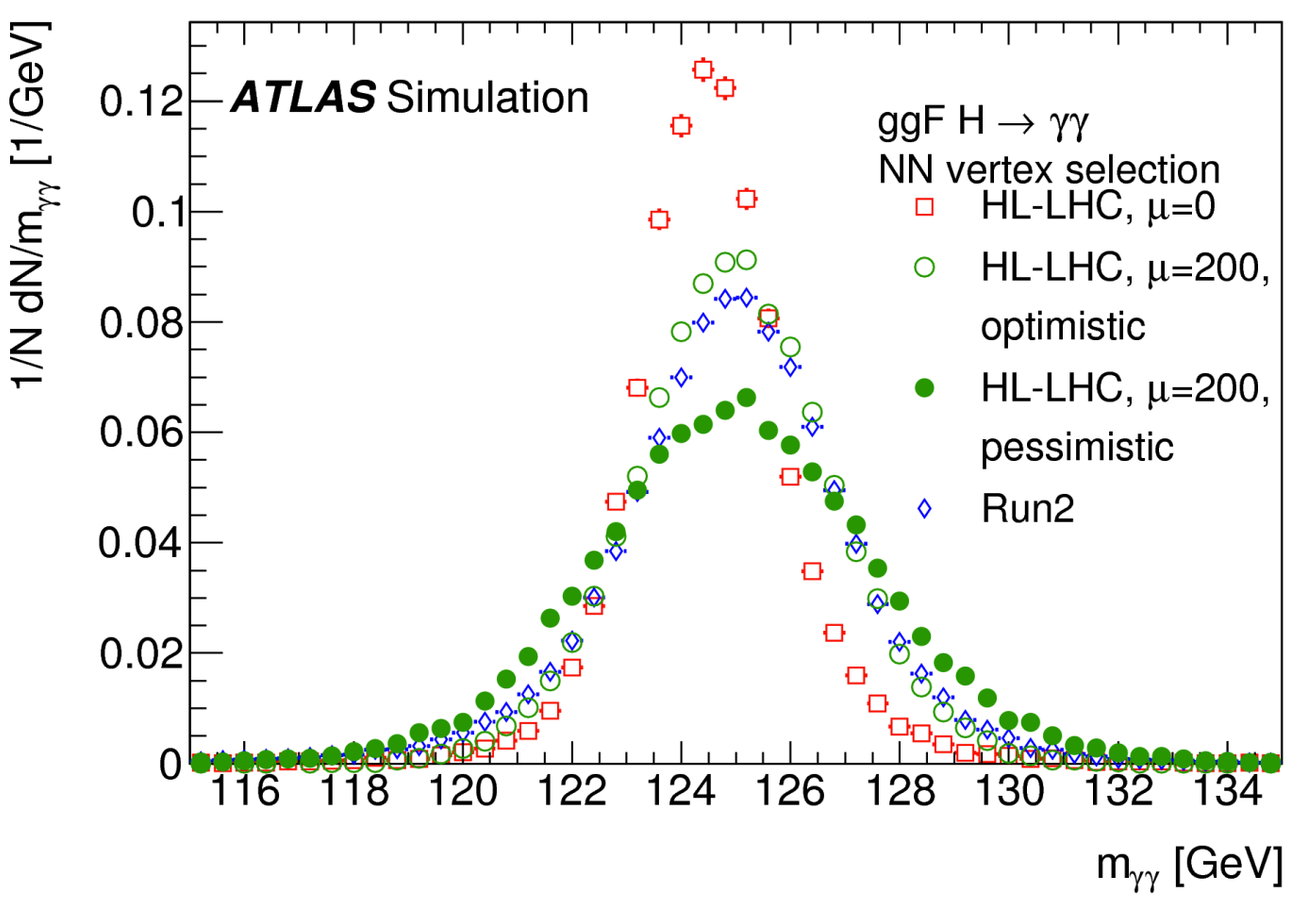
Performance Example:

Simulation shows upgraded ATLAS detector can maintain sensitivity to golden, H-> γγ channel.

Optimistic scenario: increased statistics reduce global constant term to design value, 0.7%.

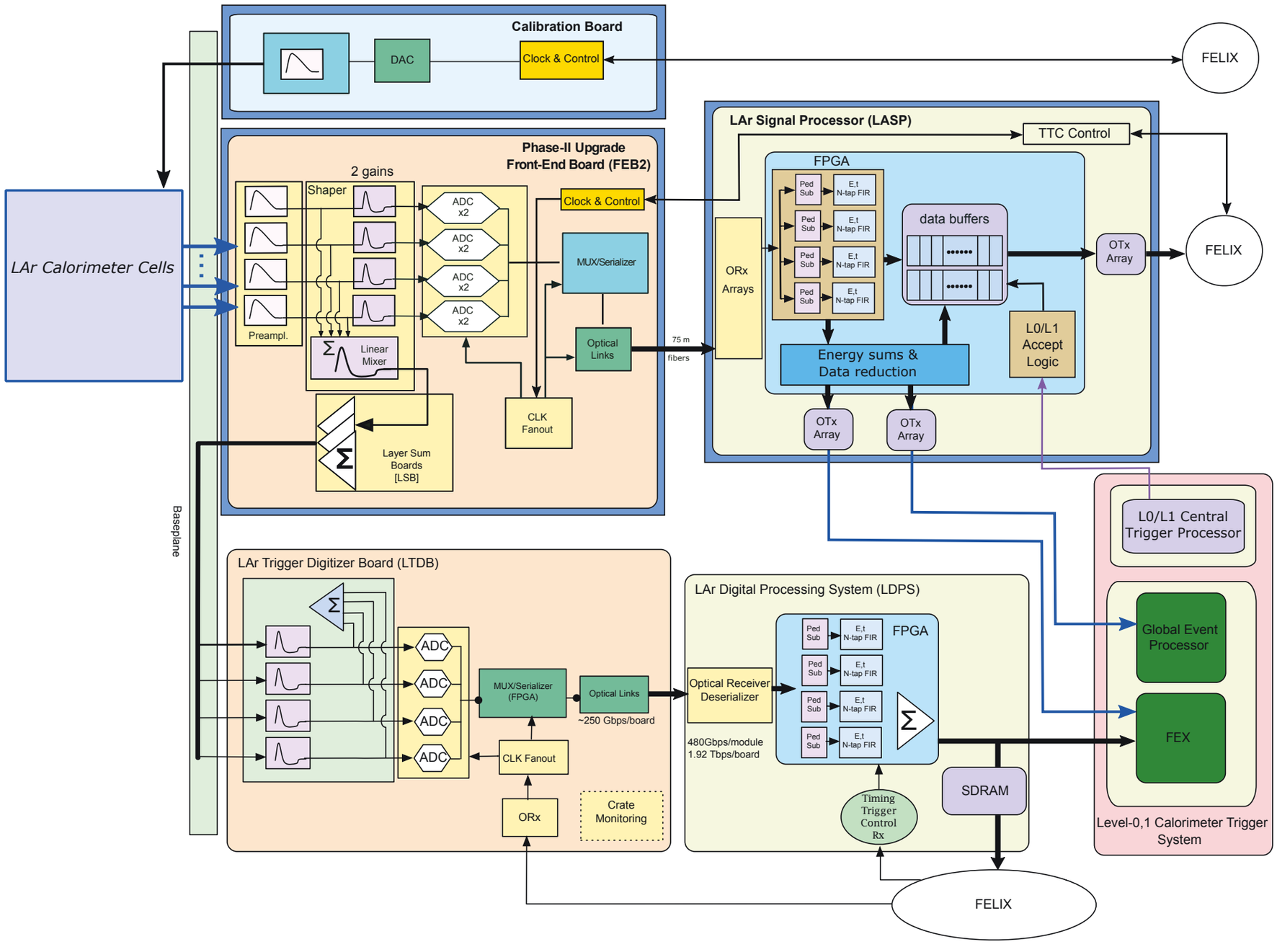
Pessimistic scenario: term remains same as 2015, 1% barrel and 1.4% endcap .

$$\frac{\sigma_E}{E} = \frac{a}{\sqrt{E}} \oplus \frac{b}{E} \oplus c$$



Phase-II Readout Electronics

Existing readout electronics will be completely replaced:



Front-End

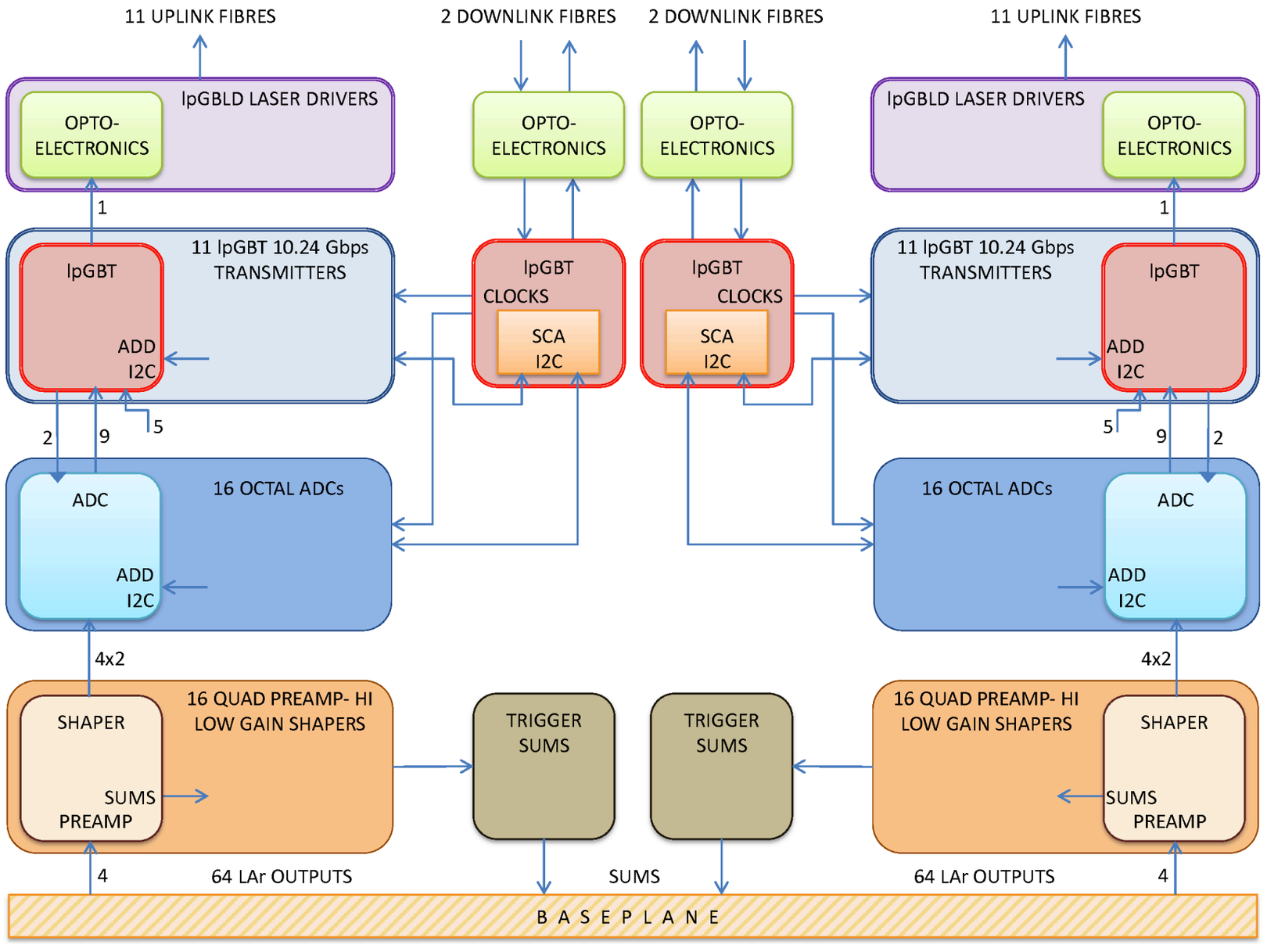
- Pulse shaping optimized to minimize total noise.
- New calibration board.
- Full granularity, each cell is digitized and sent to the backend.

Off Detector

- New, LAr Signal Processor (LASP) board to process digitized inputs and output energy and timing information.
- Information is sent from the LASP to new, L0 Triggers.

Front-End Design

The Front-end board has separate ASICs for the Preamp/Shaper, Digitization, Serialization, and Optical Transmission:



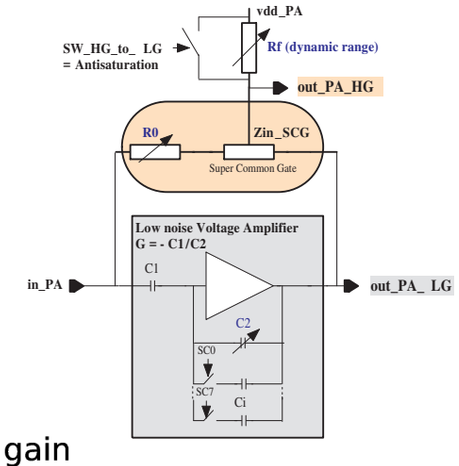
Preamplifier / Shaping ASIC

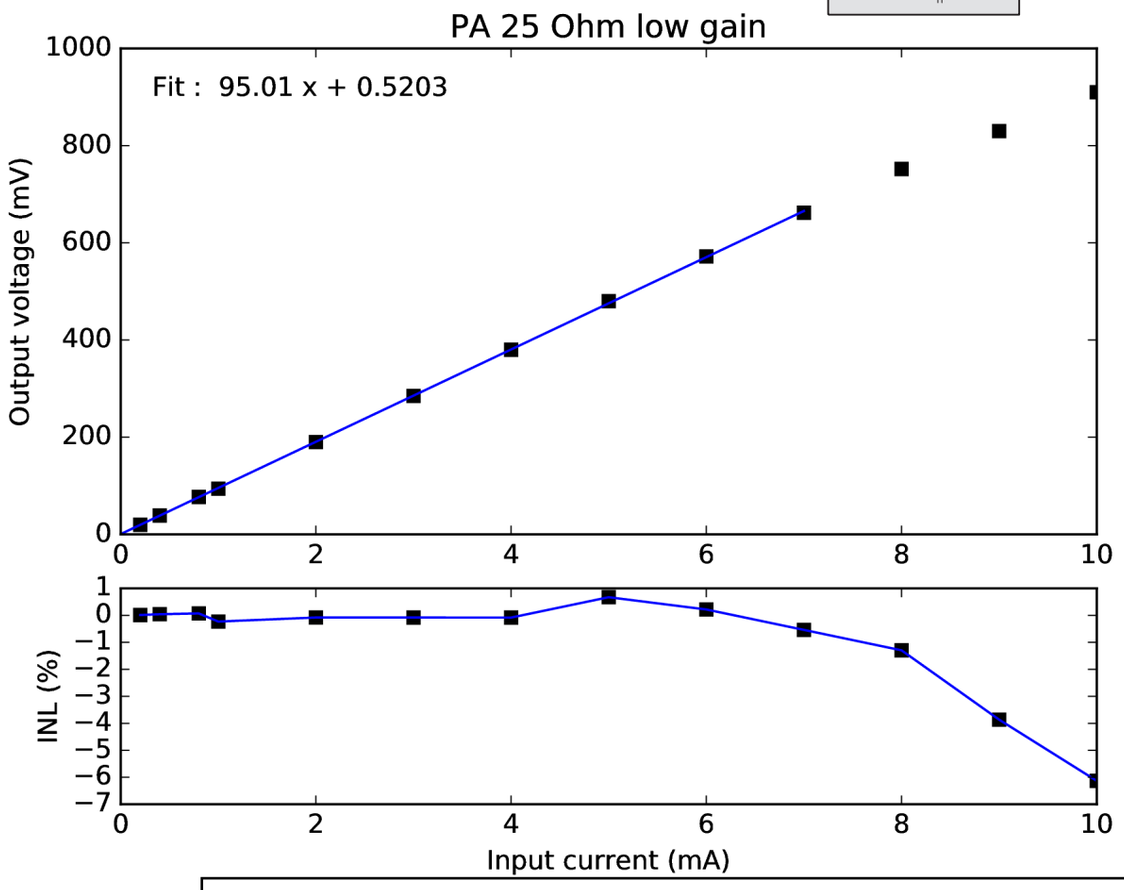
The Preamplifier and Shaping will be implemented on a single ASIC.

- 65 nm and 130 nm CMOS prototypes have both been explored.

130 nm

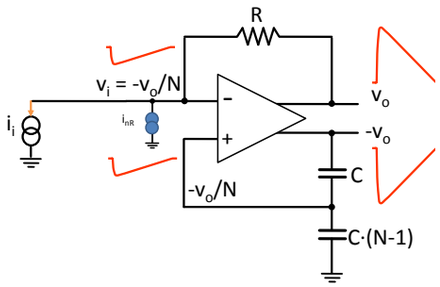
- Linearity better than 0.5%, up to 7 mA.

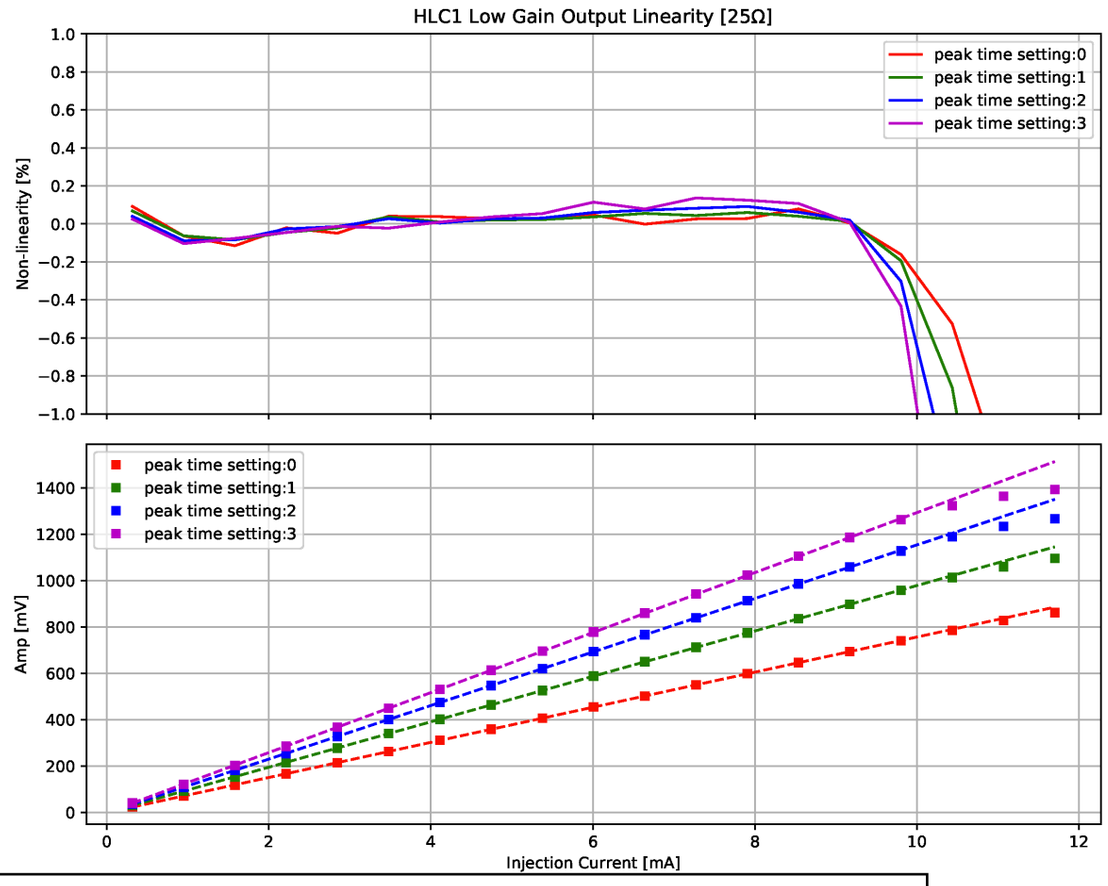




65 nm

- Linearity better than 0.2%, up to 10 mA.



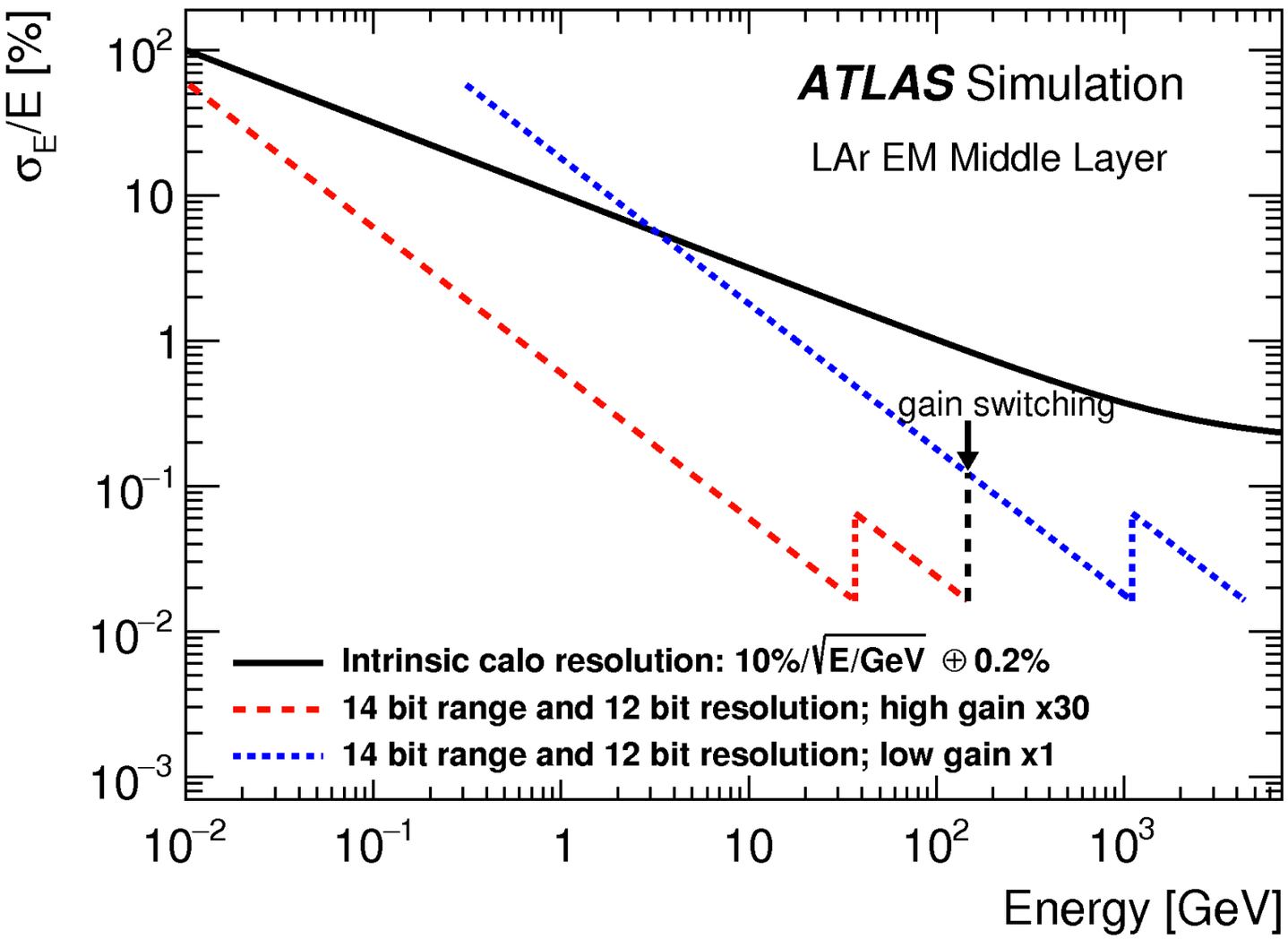


Final design will be on a 130nm chip merging aspects of both prototypes.

Digitization

The LAr cell's electronic noise must be less than MIP signal. Requiring ADC's least significant bit (LSB) value to be less than electronic noise leads to a dynamic range 16 bits wide.

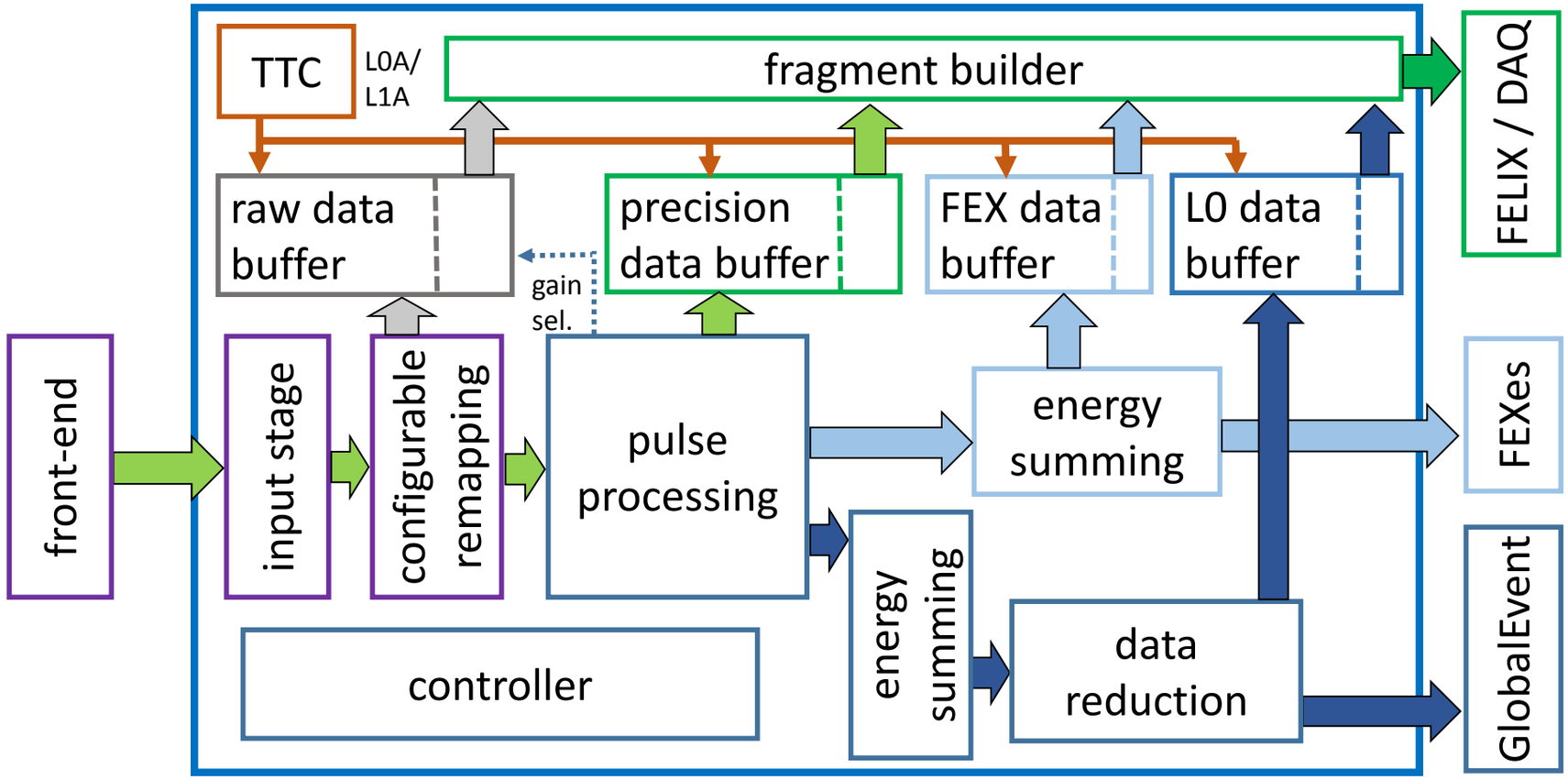
- Readout electronics utilize radiation hard,14 bit ADCs.
- To cover 16 bit range a two gain system is utilized.
- Energy of gain switching chosen so photons from H→γγ, have the same gain as electrons from Z→ee (used for energy scale calibration.)



LASP

In the back-end, Phase-II Upgrade introduces new LAr Signal Processor (LASP) based on FPGA technology:

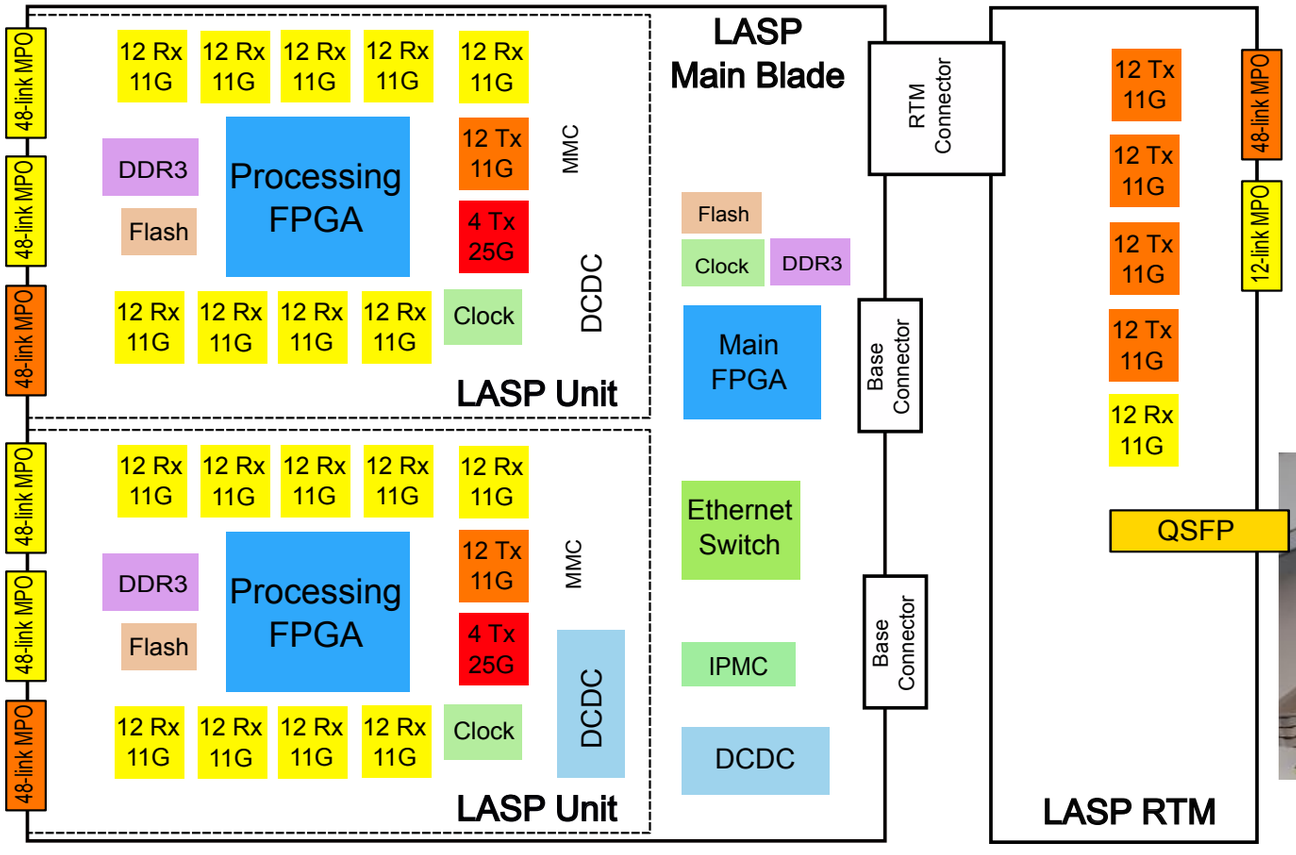
- Processes digitized waveforms from each of the calorimeter cells.
- Digital filtering algorithms to calculate energy and timing of LAr pulse.
- Interfaces to lowest level trigger (L0), hardware triggers and Data Acquisition (DAQ).
- Buffer data while awaiting trigger decision.



LASP Module

Each LASP module contains two LASP units each with it's own processing FPGA:

- LASP board design is based on Advanced Telecommunication Computing Architecture (ACTA)
- Each unit includes elector-optical receiver and transceiver arrays.
- FPGA takes inputs from up to 4 FEBs, covering 448-512 calorimeter cells.
- A test board is being developed based on the Intel Stratix 10 FPGA.



Desire reliability: so LASP processors will not need to be replaced over 10+ years of operation.

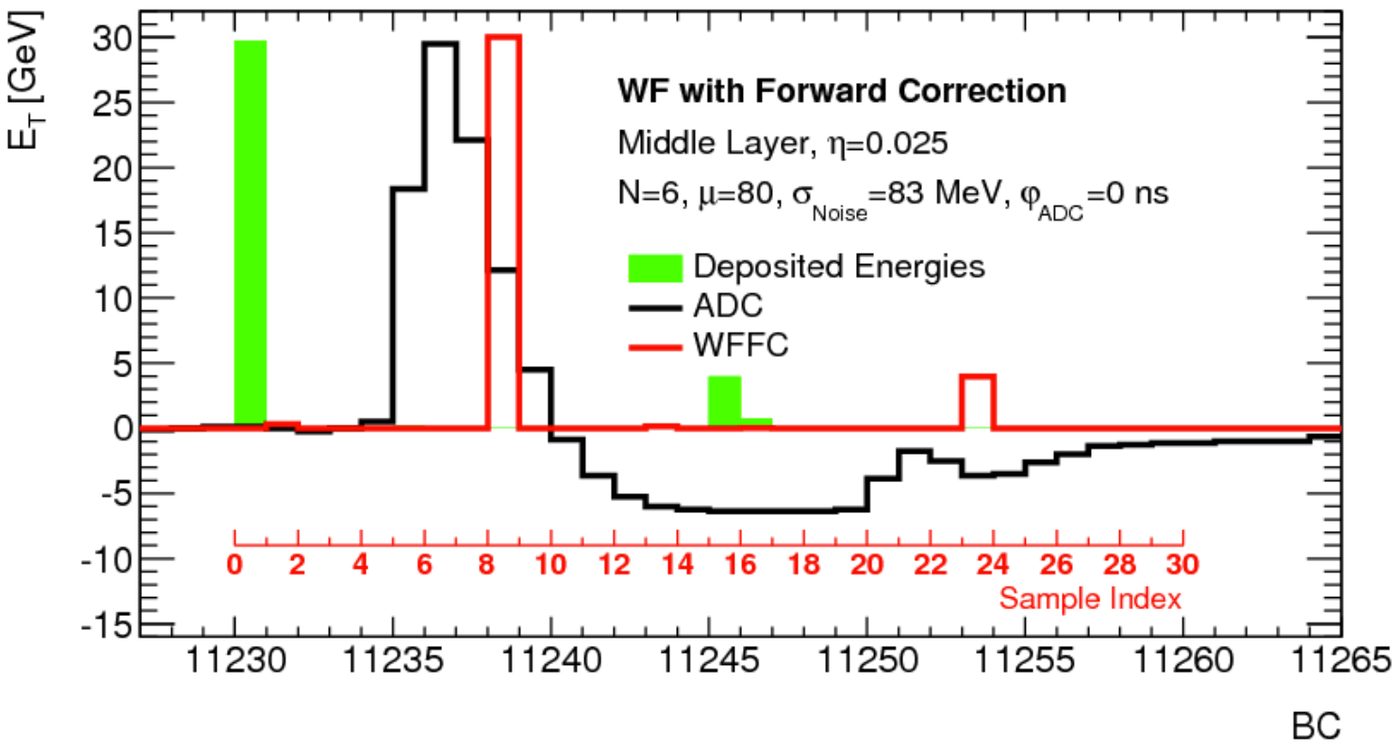
Stratix 10 Development Kit

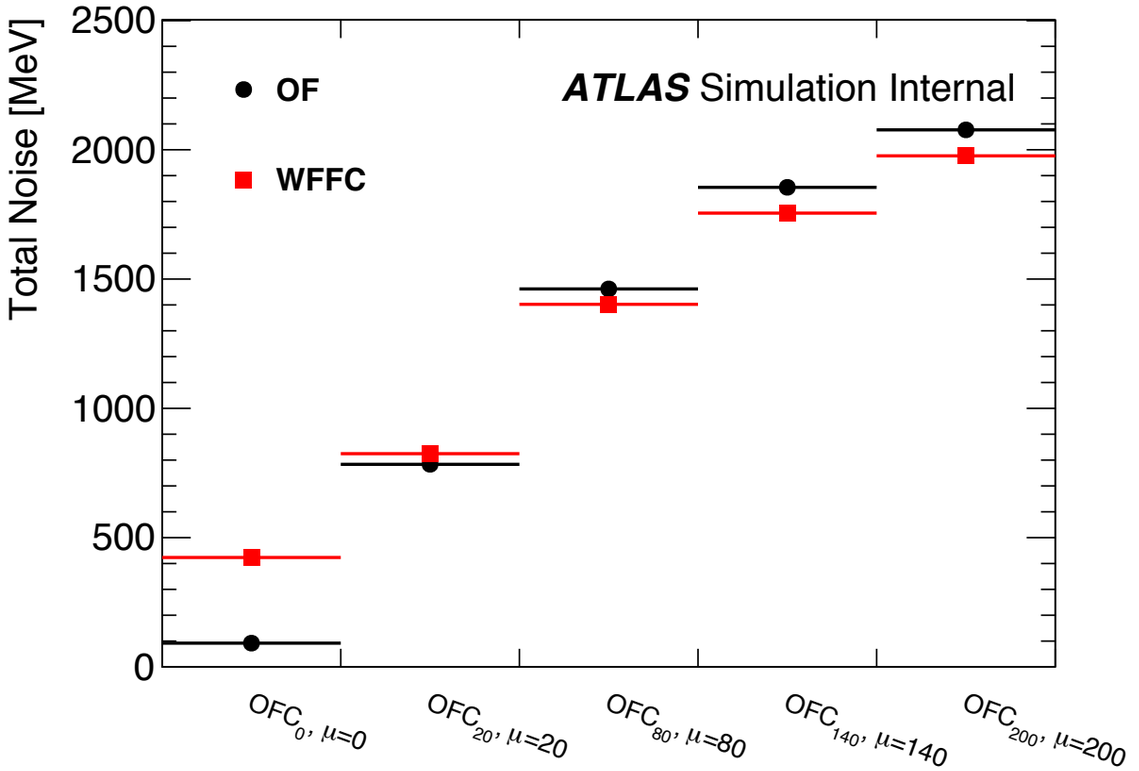
Digital Filtering Algorithms

- Current digital filtering algorithm uses **optimal filtering coefficients (OFC)**, to extract each cell's energy and timing information.
- In some cases, other algorithms such as the **Wiener Filter**, may better suppress the pileup noise. Studies are ongoing.

*Only 4 samples used since Run-2

OFC

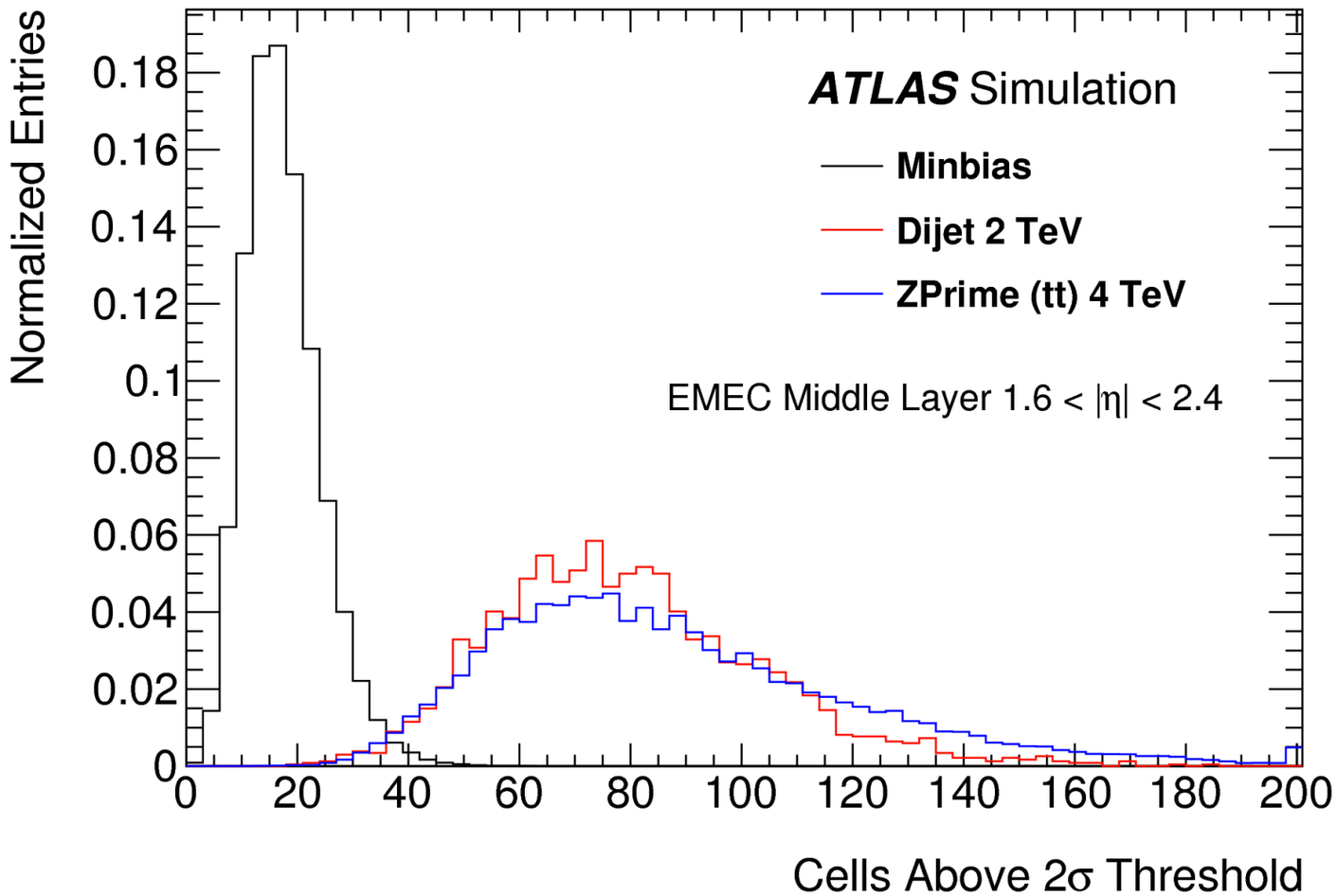




Trigger Bandwidth

LAr Calorimeter interfaces with the L0 (L1) triggers:

- Data bandwidth and links to the FPGA depends on the number of cells transmitted to the trigger.
- For the L0 global trigger, an energy threshold of 2 times the cell noise, 2σ, is applied.
- For 2σ threshold ~5.5% of cells are normally transmitted.
- However, high energy particles or noise bursts can cause individual FPGAs to transmit a significantly greater fraction of cells.
- Planned bandwidth sufficient to transmit 30% of cells, ~153.
- Also requires bit pattern (512 bits) reflecting which cells are above threshold.



- Bandwidth per LASP to L0 Global Trigger is expected to be 102.4 Gbps. (372 LASPs)

Conclusion

Beyond the Phase-I Upgrades and Run 3 the LAr Calorimeter will remain critical to ATLAS physics during the HL-LHC. In preparation for the full-replacement of the LAr Readout Electronics:

- A Technical Design Report of the LAr Phase-II Upgrades has been prepared. [LHCC Approved Project]
- Tests of first prototype front-end components.
- Simulation of off-detector readout and expected LAr Calorimeter performance.
- Results are guiding new ASIC design and test board construction.
- Target is for system installation during 2024-2025 of LS3.